PATENT
Attorney Docket No. 401148/SAKAI

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

SEIJI MATSUMOTO

Art Unit: Unknown

Application No.: Unknown

Examiner: Unknown

Filed: April 2, 2001

For: SLICING CIRCUIT

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of the above-identified patent application, please enter the following amendments and consider the following remarks.

IN THE DRAWINGS:

The Examiner is requested to approve the changes to Figure 1 as indicated in the attached Request for Approval of Drawing Amendments.

IN THE SPECIFICATION:

Replace the paragraph beginning at page 1, line 25 with:

Fig. 6 shows a sampling of a composite video signal when extracting the character broadcasting data. An example of a sampling in a one-bit data width is shown. Referring to Fig. 6, t1 to t4 are timings of a sampling respectively (hereinafter to be referred to as a sampling timing), and sampling values at these timings become x1 to x4.

Replace the paragraph beginning at page 2, line 17 with:

In the following one bit, N to N+3 become sampling points. N+4 becomes a sampling point at the next bit. A sampling operation is repeated continuously in this way.

Replace the paragraph beginning at page 4, line 12 with:

Fig. 9 is a diagram showing a result of an arithmetic processing when distortion has occurred in the input waveform of the conventional arithmetic and logic unit. A distortion of the input waveform occurs when the reception status is aggravated by a weak electric field or a ghost. Referring to Fig. 9, the value of the sampling point that has been judged as "0" in Fig. 8 is judged as "1" as a result of a correction processing, as the value becomes larger than the slice level.

Replace the paragraph beginning at page 4, line 21

According to the slicing circuit provided with the conventional arithmetic and logic unit, the sampling data is distorted. Therefore, there arises such a situation that a result of an arithmetic processing that should actually be decided as "0" is erroneously decided as "1". This has resulted in an erroneous operation.

Replace the paragraph beginning at page 8, line 15 with:

Fig. 3 is a diagram showing a result of an arithmetic processing when a distortion has occurred in the input waveform to a digital arithmetic and logic unit in the slicing circuit according to the first embodiment.

Replace the paragraph beginning at page 8, line 22 with:

Fig. 5 is a diagram showing a result of an arithmetic processing when a distortion has occurred in the input waveform to a digital arithmetic and logic unit in the slicing circuit according to the second embodiment.

Replace the paragraph beginning at page 9, line 1 with:

Fig. 6 is a diagram showing a sampling example in a one-bit data width for explaining a conventional arithmetic and logic unit.

IN THE CLAIMS:

Replace the indicated claims with:

1. (Amended) A slicing circuit comprising:

a control recording unit which exchanges data with a data bus;

a memory which temporarily stores character broadcasting data extracted from the data bus;

an analog-to-digital (A/D) converter which receives a composite video signal and converts the composite video signal into digital values;

a digital arithmetic and logic unit which receives the digital values converted by the A/D converter, calculates character broadcasting data, and outputs the character broadcasting data to the memory;

a SYNC separator which receives the composite video signal, and extracts a vertical or horizontal synchronizing signal;

a clock generating unit; and

a timing control circuit which receives the outputs of the SYNC separator, the clock generating unit, and the control recording unit, outputs to the memory and the digital arithmetic and logic unit, and controls timing.

2. (Amended) The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes:

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs first, second, third, and fourth control signals that show timing in a one-bit data width;

a first integrator connected to one of the plurality of latch circuits and receiving the second control signal;

a second integrator connected to one of the latch circuits to which the first integrator is not connected, the second integrator receiving the third control signal;

a first adder which receives the outputs of the first and second integrators;

a third integrator connected to one of the latch circuits to which the first and second integrators are not connected, the third integrator receiving the first control signal;

a second adder which receives the outputs of the third integrator and the first adders; and

a correcting circuit which receives the outputs of the second adder and the fourth control signal.

3. (Amended) The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs first and second control signals that show timing in a one-bit data width;

a first selector connected to at least two of the latch circuits and receiving the first control signal;

a second selector connected to at least two of the latch circuits to which the first selector is not connected, the second selector receiving the second control signal;

a first adder which receives the outputs of the first and second selectors;

an integrator connected to at least two of the latch circuits to which the first and second selectors are not connected;

a second adder which receives the outputs of the integrator and the first adder; and

a correcting circuit which receives the output of the second adder.

4. (Amended) A slicing circuit for arithmetically correcting character broadcasting data extracted from a composite video signal, the slicing circuit comprising an arithmetic processing unit switching arithmetic processing at a sampling timing of the composite video signal.

IN THE ABSTRACT:

Replace the Abstract with:

ABSTRACT OF THE DISCLOSURE

A slicing circuit is provided with a data bus, a control register, a text RAM, a digital arithmetic and logic unit, a timing control circuit, an A/D converter, a SYNC separator, and a PLL circuit.

REMARKS

The foregoing Amendment improves the form of the application without adding new matter.

Respectfully submitted,

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SPECIFICATION, CLAIMS AND ABSTRACT AS PRELIMINARILY AMENDED

Amendments to the paragraph beginning at page 1, line 25:

Fig. 6 shows a sampling of a composite video signal when extracting the character broadcasting data. An example of a sampling in a ~~data~~ one-bit data width is shown. Referring to Fig. 6, t1 to t4 are timings of a sampling respectively (hereinafter to be referred to as a sampling timing), and sampling values at these timings become x1 to x4.

Amendments to the paragraph beginning at page 2, line 17:

In the following one bit, N to N+3 become sampling points. N+4 becomes a sampling point at the next ~~one~~ bit. A sampling operation is repeated continuously in this way.

Amendments to the paragraph beginning at page 4, line 12:

Fig. 9 is a diagram showing a result of an arithmetic processing when ~~a~~ distortion has occurred in the input waveform ~~by~~ of the conventional arithmetic and logic unit. A distortion of the input waveform occurs when the reception status is aggravated by a weak electric field or a ghost. Referring to Fig. 9, the value of the sampling point that has been judged as "0" in Fig. 8 is judged as "1" as a result of a correction processing, as the value becomes larger than the slice level.

Amendments to the paragraph beginning at page 4, line 21

According to the slicing circuit provided with the conventional arithmetic and logic unit, the sampling data is distorted. Therefore, there arises such a situation that a result of an arithmetic processing that should actually be decided as "0" is erroneously decided as "1". This has resulted in ~~a cause of~~ an erroneous operation.

Amendments to the paragraph beginning at page 8, line 15:

Fig. 3 is a diagram showing a result of an arithmetic processing when a distortion has occurred in the input waveform ~~by~~ to a digital arithmetic and logic unit in the slicing circuit according to the first embodiment.

Amendments to the paragraph beginning at page 8, line 22:

Fig. 5 is a diagram showing a result of an arithmetic processing when a distortion has occurred in the input waveform ~~by~~ to a digital arithmetic and logic unit in the slicing circuit according to the second embodiment.

Amendments to the paragraph beginning at page 9, line 1:

Fig. 6 is a diagram showing a sampling example in a ~~data~~ one-bit data width for explaining a conventional arithmetic and logic unit.

Amendments to existing claims:

1. (Amended) A slicing circuit comprising:

a control recording unit which exchanges data with a data bus;

a memory which temporarily stores character broadcasting data extracted from the data bus;

an analog-to-digital (A/D) converter which receives a composite video signal~~,~~ and converts the composite video signal into digital values;

a digital arithmetic and logic unit which receives the digital values converted by the A/D converter, calculates character broadcasting data, and outputs the character broadcasting data to the memory;

a SYNC separator which receives the composite video signal, and extracts a vertical or horizontal synchronizing signal;

a clock generating unit; and

a timing control circuit which receives the ~~output~~ outputs of the SYNC separator, the clock generating unit, and the control recording unit, ~~output~~ outputs to the memory and the digital arithmetic and logic unit, and controls ~~a~~ timing.

2. (Amended) The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes ~~;~~:

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs ~~a~~ first ~~through~~, second, third, and fourth control signals that show ~~a~~ timing in a one-bit data width;

a first integrator connected to one of the plurality of latch circuits ~~, which first integrator receives~~ and receiving the second control signal;

a second integrator connected to ~~a~~ one of the latch ~~circuit,~~ circuits to which the first integrator is not connected, ~~out of the plurality of latch circuits, which~~ the second integrator ~~receives~~ receiving the third control signal;

a first adder which receives the ~~output~~ outputs of the first and second integrators;

a third integrator connected to ~~a~~ one of the latch ~~circuit,~~ circuits to which the first and second integrators are not connected, ~~out of the plurality of latch circuits, which~~ the third integrator ~~receives~~ receiving the first control signal;

a second adder which receives the ~~output~~ outputs of the third integrator and the first adders; and

a correcting circuit which receives the ~~output~~ outputs of the second adder and the fourth control signal.

3. (Amended) The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs ~~a~~ first ~~through fourth~~ and second control signals that show ~~a~~ timing in a one-bit data width;

a first selector connected to at least two of the latch circuits ~~out of the plurality of latch circuits, which first selector receives~~ and receiving the first control signal;

a second selector connected to at least two of the latch circuits, ~~;~~ to which the first selector is not connected, ~~out of the plurality of latch circuits, which~~ the second selector ~~receives~~ receiving the second control signal;

a first adder which receives the ~~output~~ outputs of the first and second selectors;

an integrator connected to at least two of the latch circuits, ~~;~~ to which the first and second selectors are not connected ~~, out of the plurality of latch circuits~~;

a second adder which receives the ~~output~~ outputs of the integrator and the first adder; and

a correcting circuit which receives the output of the second adder.

4. (Amended) A slicing circuit for arithmetically correcting character broadcasting data extracted from a composite video signal, the slicing circuit comprising ~~:~~ an arithmetic processing unit ~~which changes over an~~ switching arithmetic processing at a sampling timing of the composite video signal.

Amendments to the abstract:

ABSTRACT OF THE DISCLOSURE

~~The~~A slicing circuit is provided with a data bus ~~8~~, a control register ~~1~~, a text RAM ~~2~~, a digital arithmetic and logic unit ~~3~~, a timing control circuit ~~4~~, an A/D converter ~~5~~, a SYNC separator ~~6~~, and a PLL circuit ~~7~~.

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CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A slicing circuit comprising:

a control recording unit which exchanges data with a data bus;

a memory which temporarily stores character broadcasting data extracted from the data bus;

an analog-to-digital (A/D) converter which receives a composite video signal and converts the composite video signal into digital values;

a digital arithmetic and logic unit which receives the digital values converted by the A/D converter, calculates character broadcasting data, and outputs the character broadcasting data to the memory;

a SYNC separator which receives the composite video signal, and extracts a vertical or horizontal synchronizing signal;

a clock generating unit; and

a timing control circuit which receives the outputs of the SYNC separator, the clock generating unit, and the control recording unit, outputs to the memory and the digital arithmetic and logic unit, and controls timing.

2. The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes:

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs first, second, third, and fourth control signals that show timing in a one-bit data width;

a first integrator connected to one of the plurality of latch circuits and receiving the second control signal;

a second integrator connected to one of the latch circuits to which the first integrator is not connected, the second integrator receiving the third control signal;

a first adder which receives the outputs of the first and second integrators;

a third integrator connected to one of the latch circuits to which the first and second integrators are not connected, the third integrator receiving the first control signal;

a second adder which receives the outputs of the third integrator and the first adders; and

a correcting circuit which receives the outputs of the second adder and the fourth control signal.

3. The slicing circuit according to claim 1, wherein the digital arithmetic and logic unit includes,

a plurality of latch circuits;

an arithmetic processing control circuit which receives a sampling clock and a slicing clock, and outputs first and second control signals that show timing in a one-bit data width;

a first selector connected to at least two of the latch circuits and receiving the first control signal;

a second selector connected to at least two of the latch circuits to which the first selector is not connected, the second selector receiving the second control signal;

a first adder which receives the outputs of the first and second selectors;

an integrator connected to at least two of the latch circuits to which the first and second selectors are not connected;

a second adder which receives the outputs of the integrator and the first adder; and

a correcting circuit which receives the output of the second adder.

4. A slicing circuit for arithmetically correcting character broadcasting data extracted from a composite video signal, the slicing circuit comprising an arithmetic processing unit switching arithmetic processing at a sampling timing of the composite video signal.

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REQUEST FOR APPROVAL OF CHANGES TO THE DRAWINGS

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The Examiner is requested to approve the changes to Figure 1, as shown in red on the attached sheets of drawings.

Respectfully submitted,

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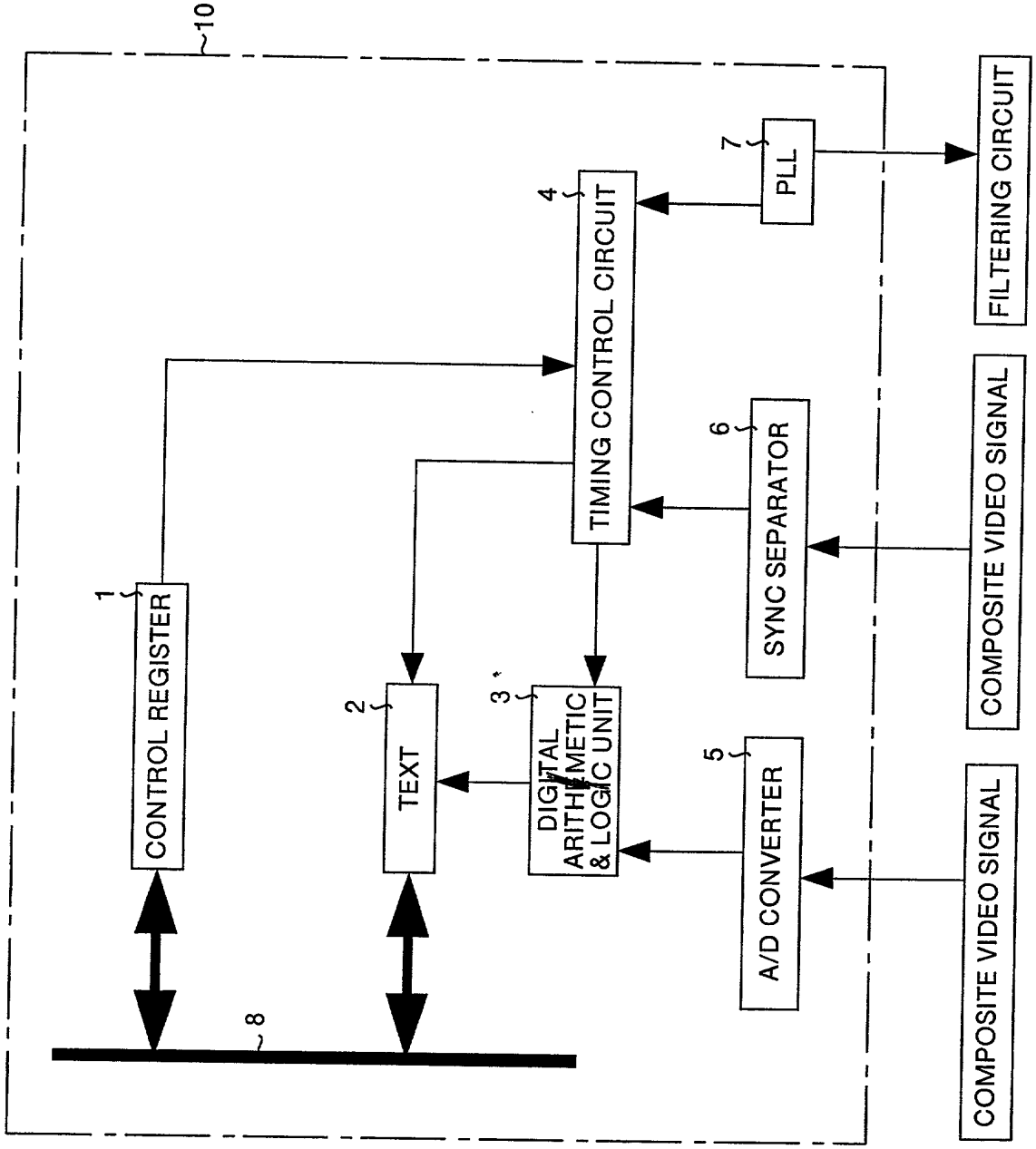
FIG.1


10
CONTROL REGISTER
1
TEXT
2
DIGITAL ARITHMETIC & LOGIC UNIT
3
TIMING CONTROL CIRCUIT
4
A/D CONVERTER
5
SYNC SEPARATOR
6
PLL
7
8
COMPOSITE VIDEO SIGNAL
COMPOSITE VIDEO SIGNAL
FILTERING CIRCUIT